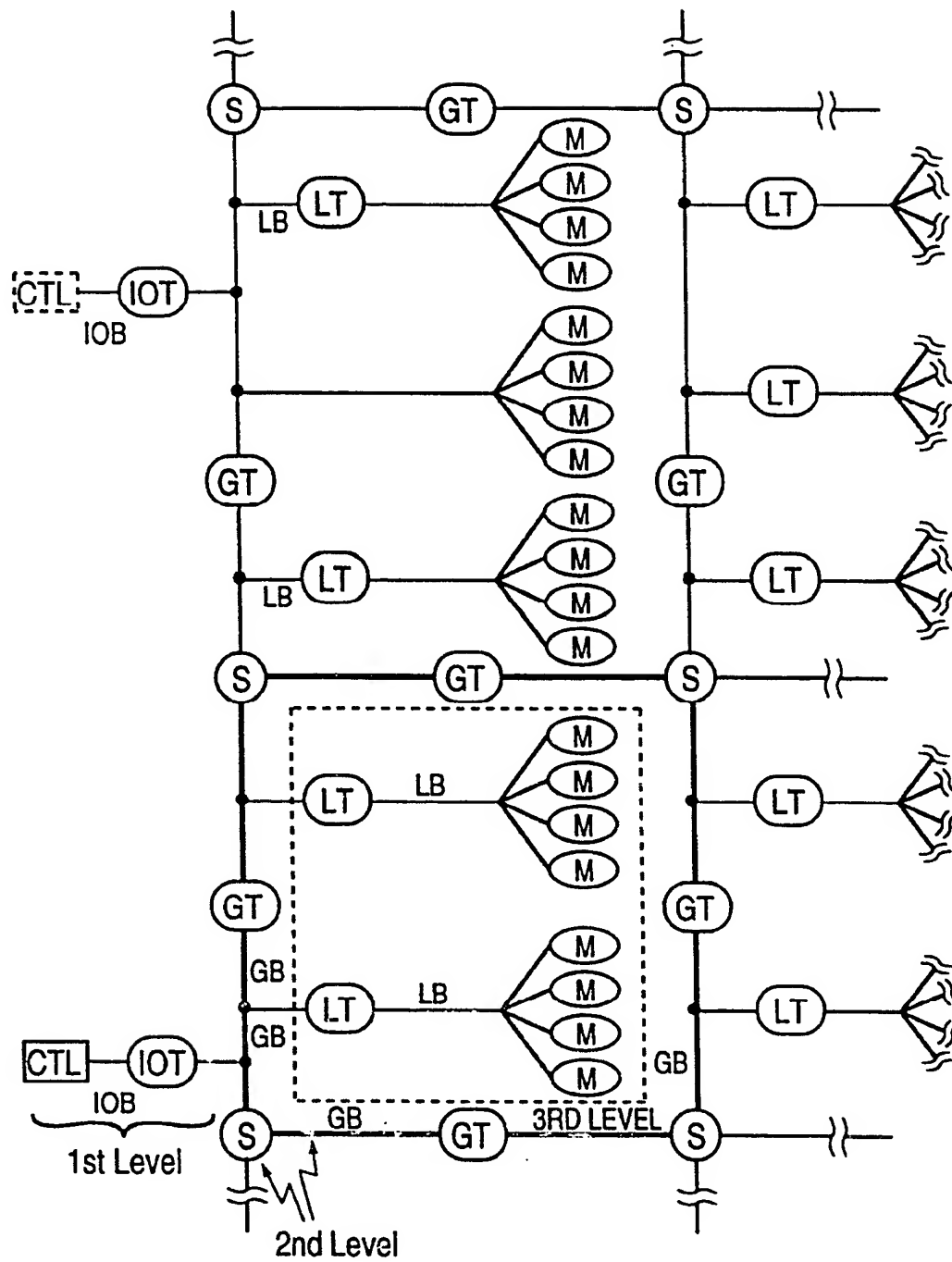


FIG. 1



- (M) - Module
 [CTL] - Controller
 [CTL] - Possible Site for Controller

FIG. 2

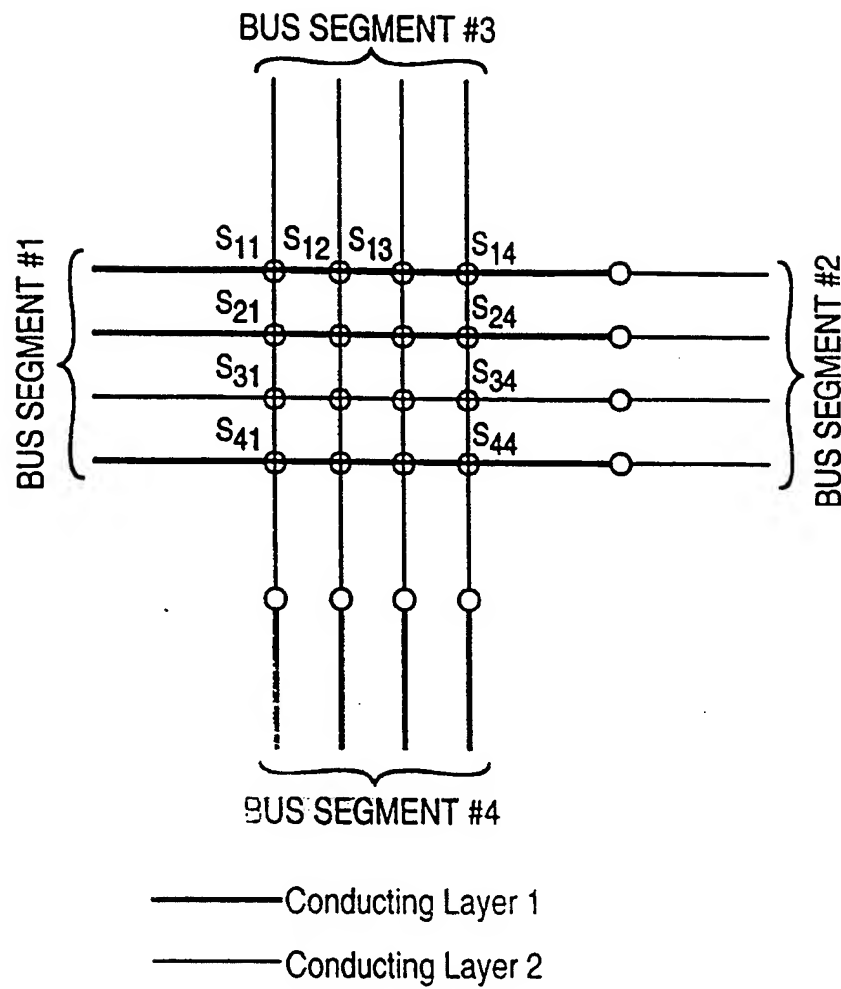


FIG. 3

Group 1 - Block - mode transfer signals

- Bus Data [0:8]
- Clk

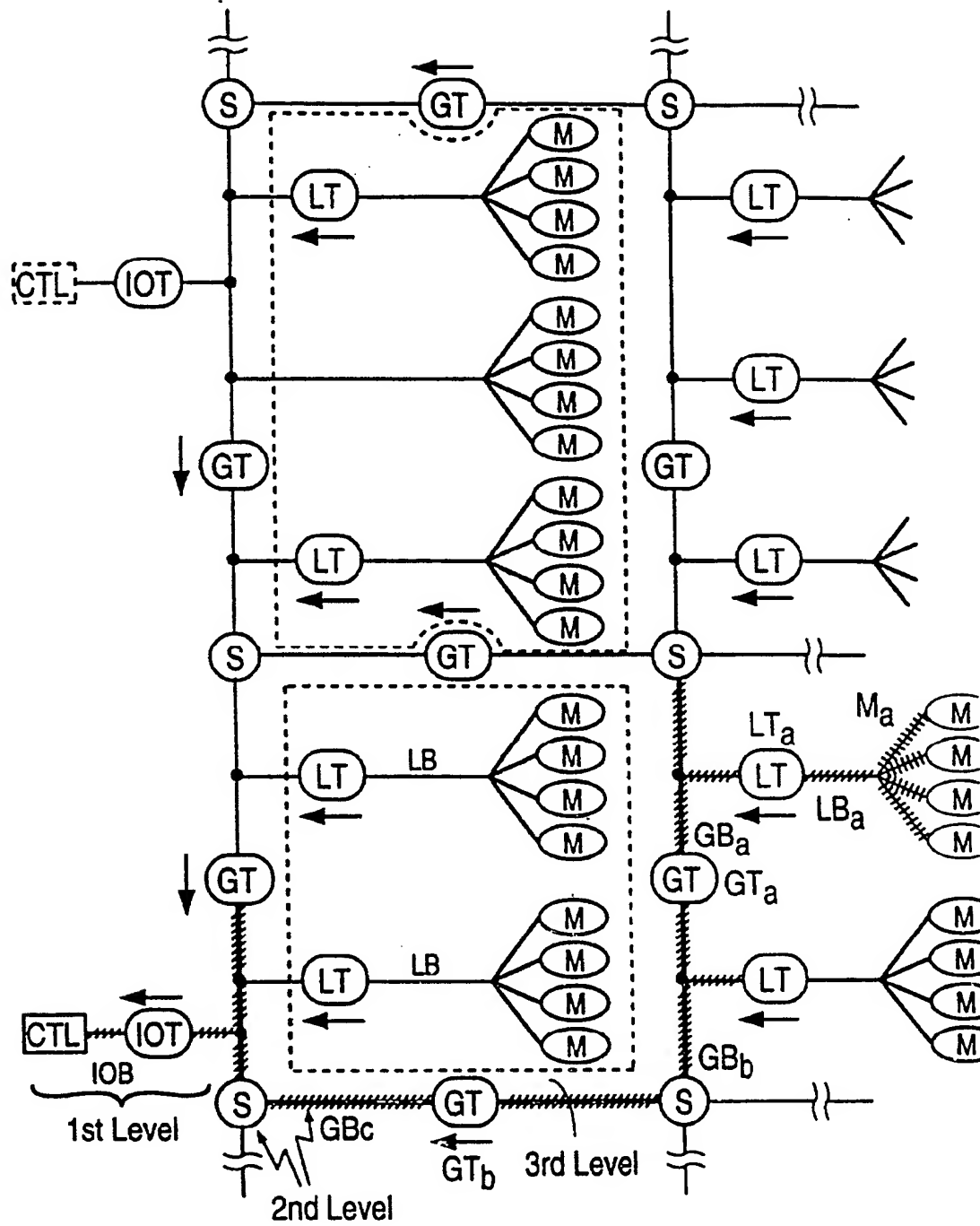
Group 2 - Asynchronous control signals

- Bus Busy (BB#)
- Transmit / Receive (T / R)
- TriState Control (TC#)

FIG. 4

BB#	T/R	TC#	BUS STATE
0	0	0	Hi Z
0	0	1	Receive
0	1	0	Hi Z
0	1	1	Transmit
1	0	0	} Idle
1	0	1	
1	1	0	
1	1	1	

FIG. 5



- (M) - Module
- [CTL] - Controller
- [CTL] - Possible Site for Controller

FIG. 6

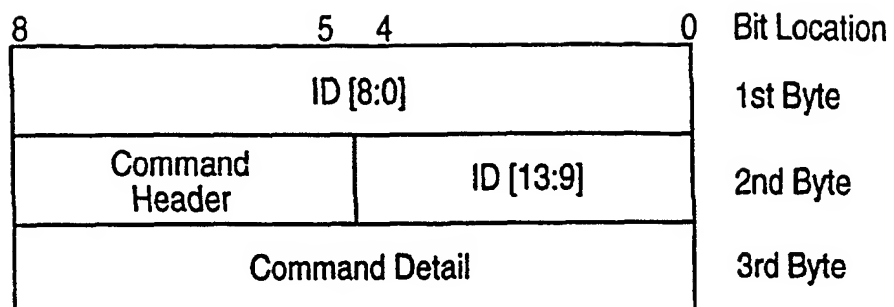


FIG. 7

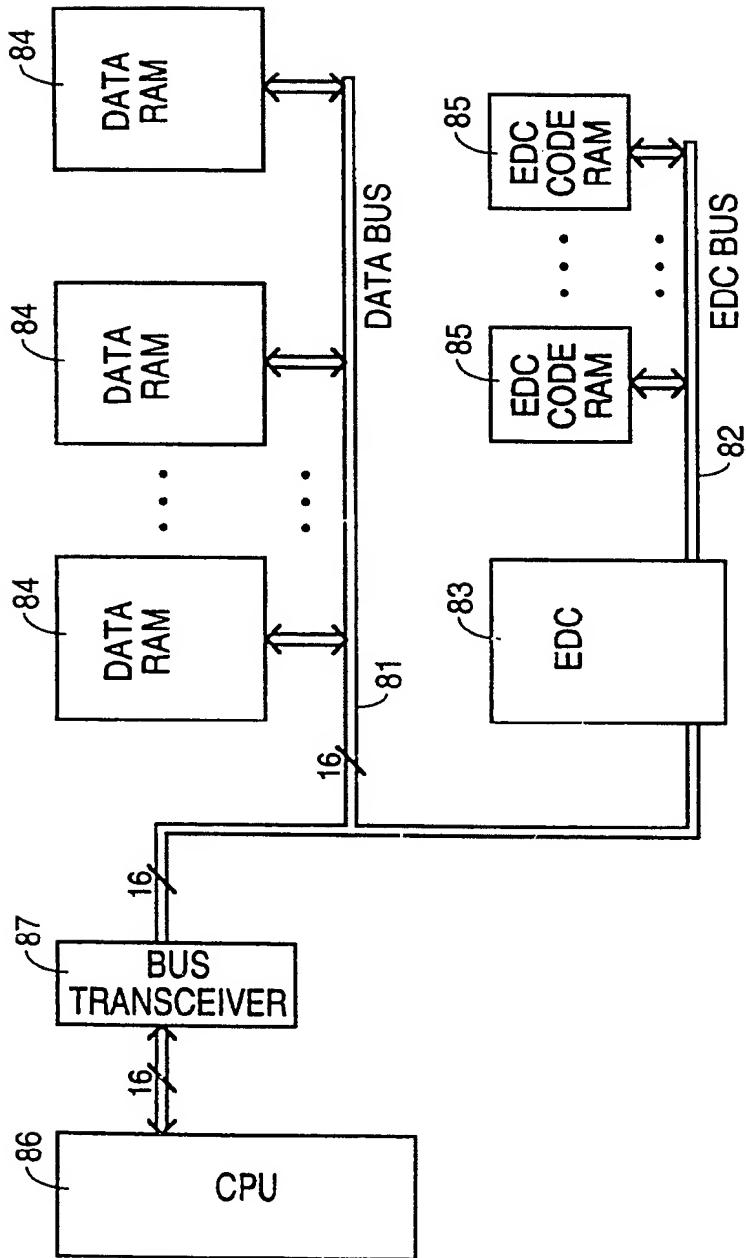


FIG. 8

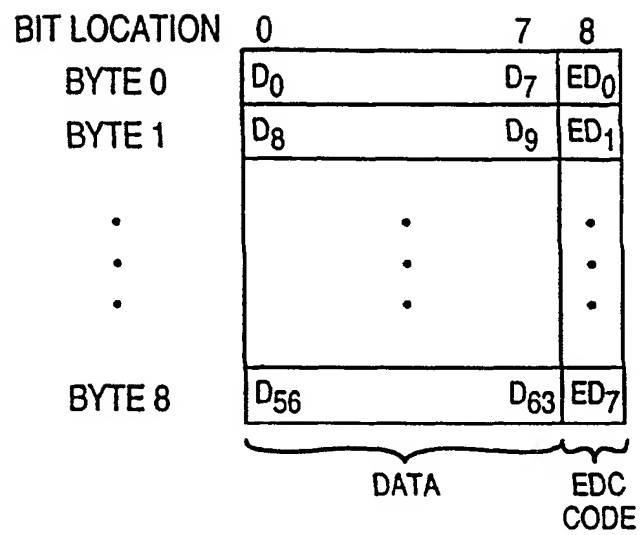


FIG. 9

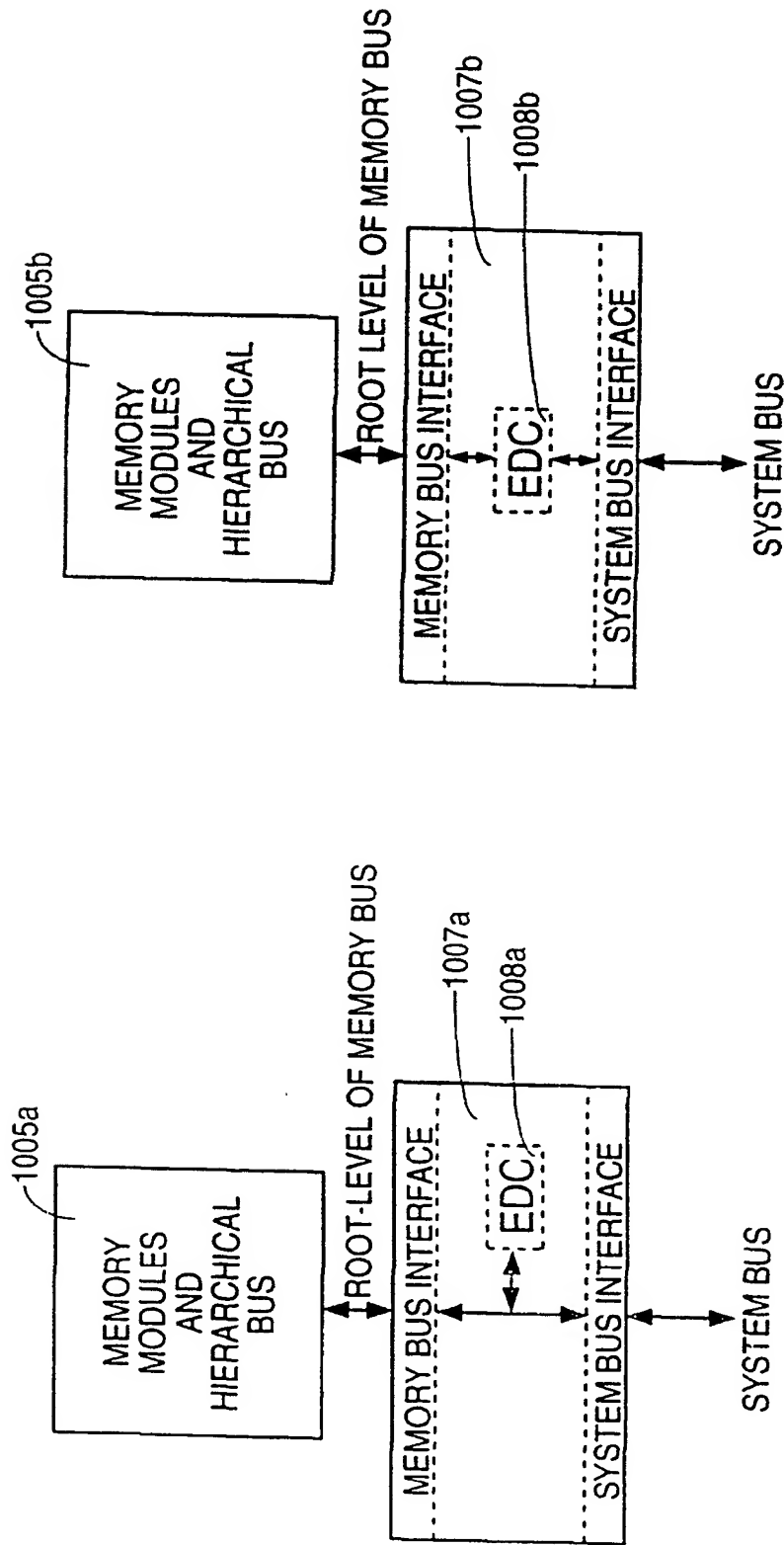


FIG. 10B

FIG. 10A

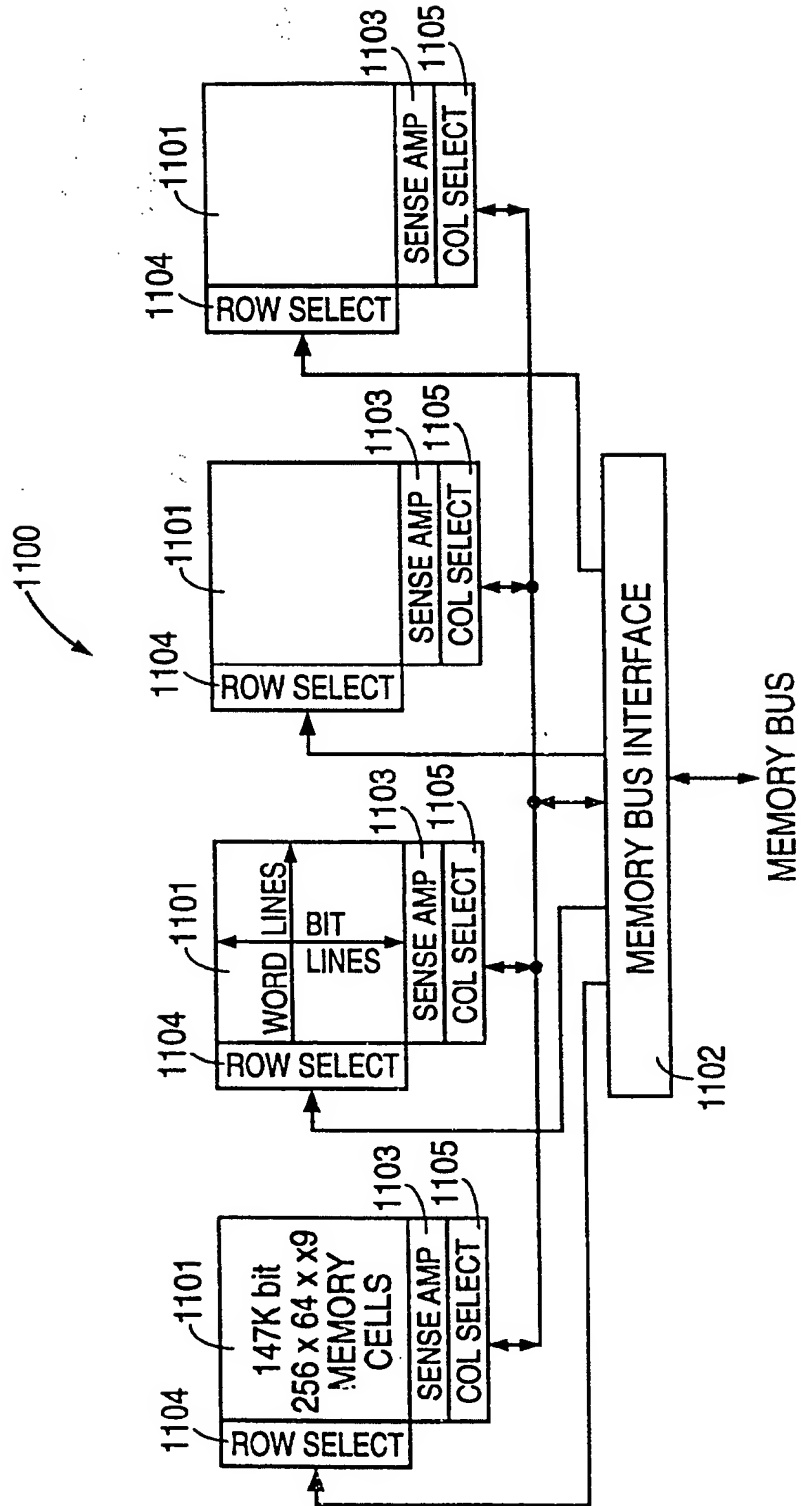


FIG. 11

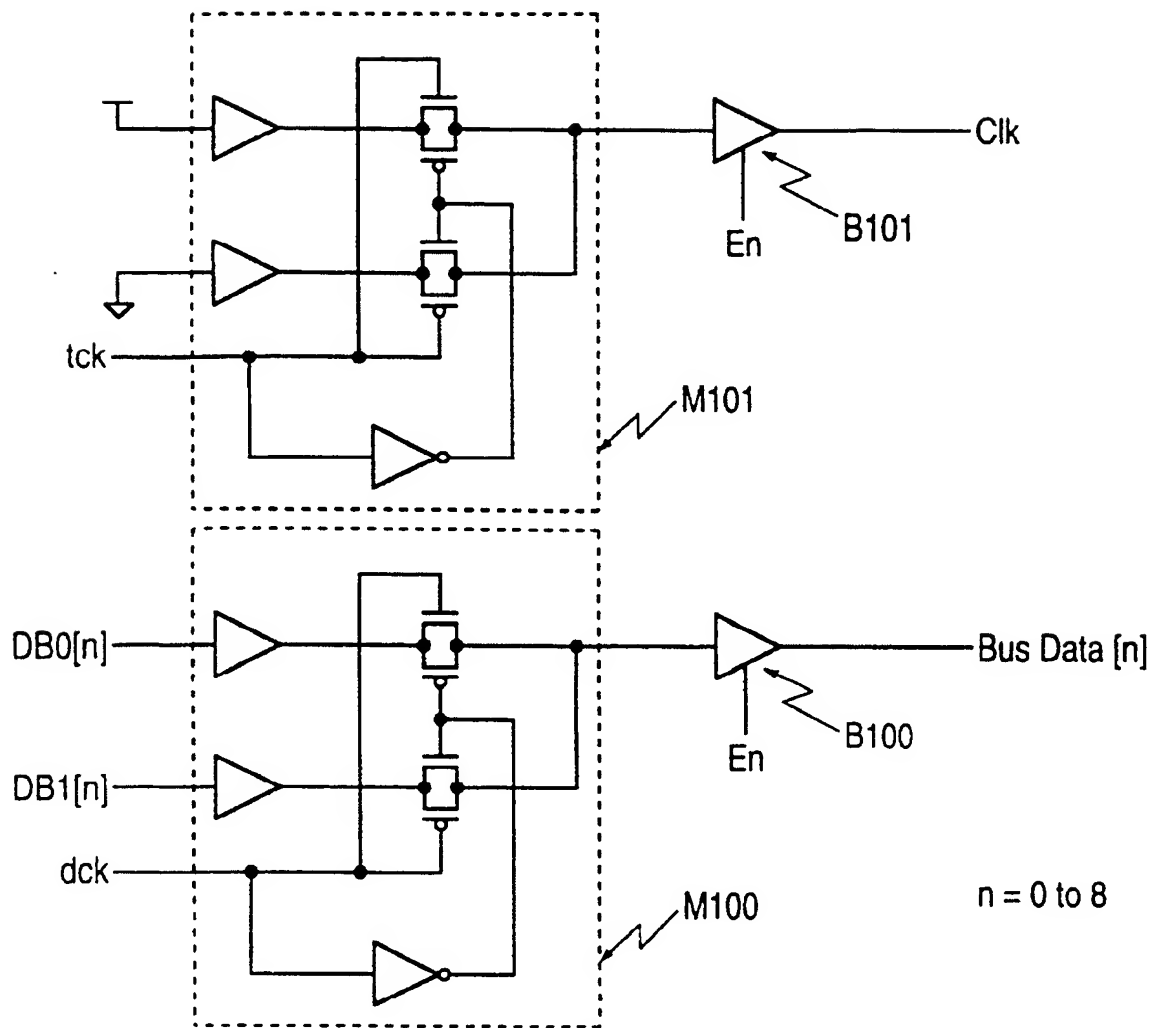


FIG. 12A

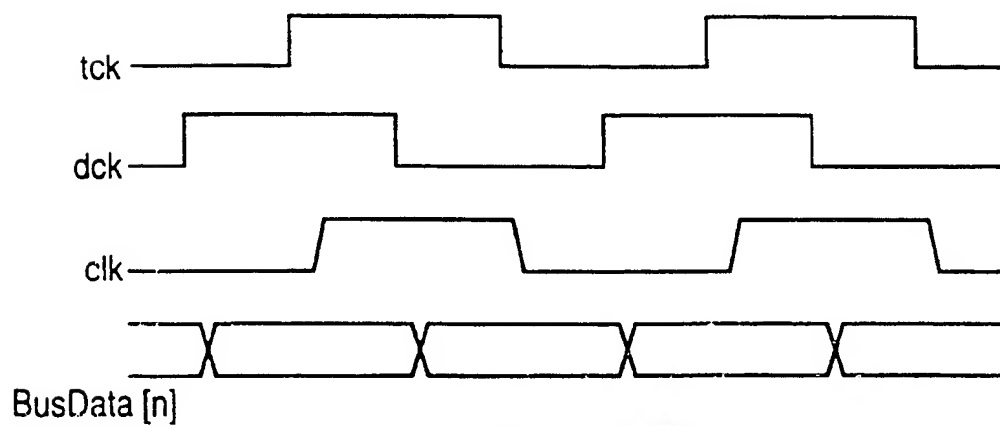


FIG. 12B

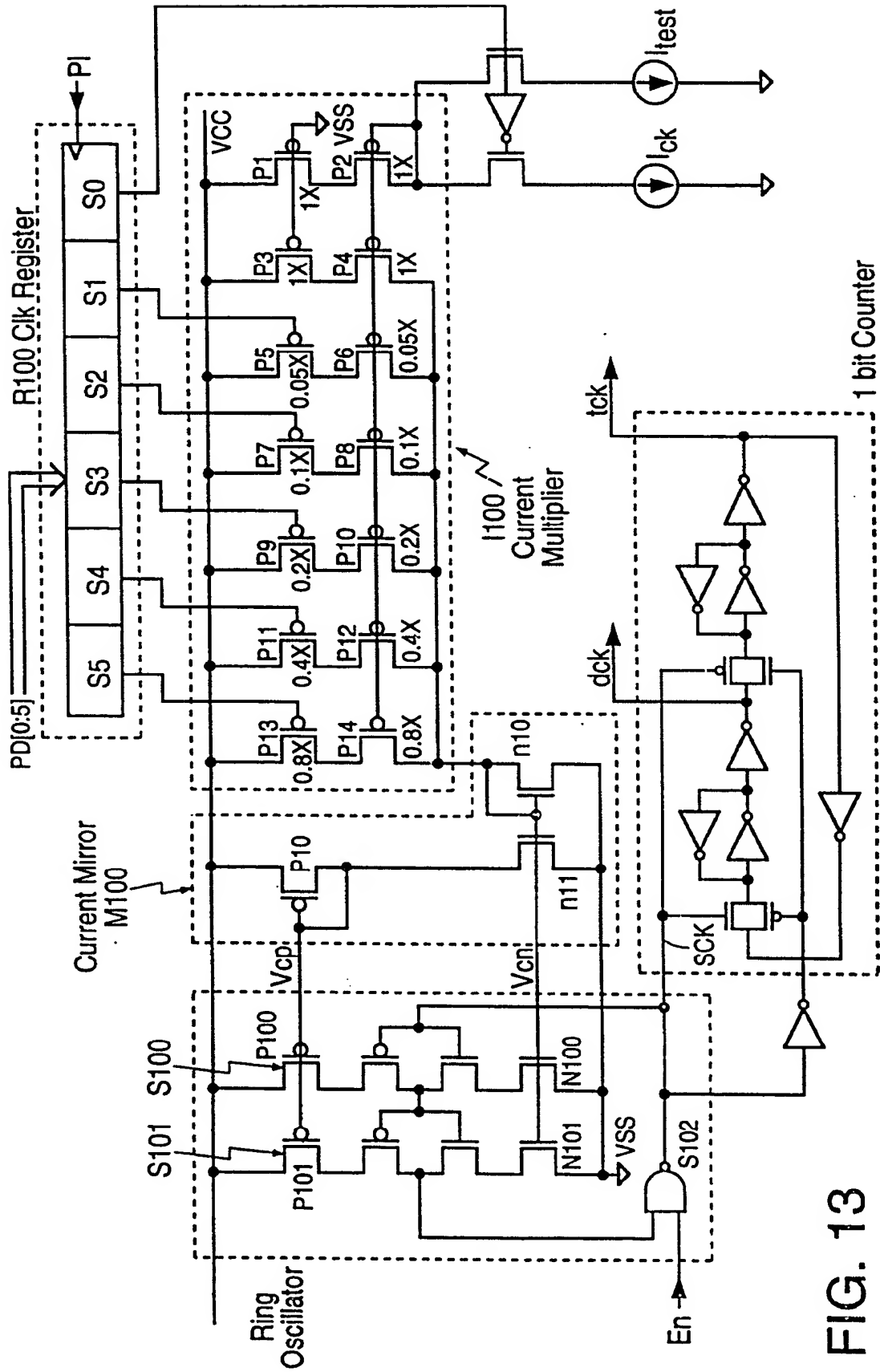
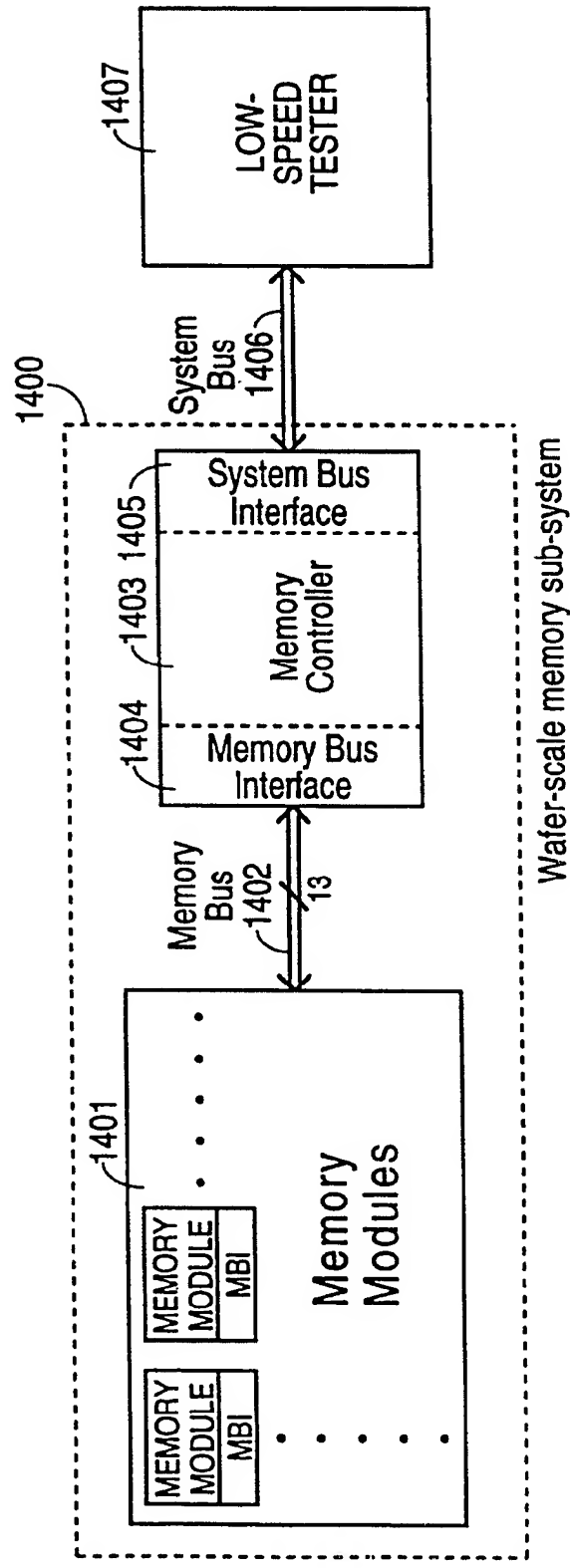


FIG. 13



MBI = Memory Bus Interface

FIG. 14

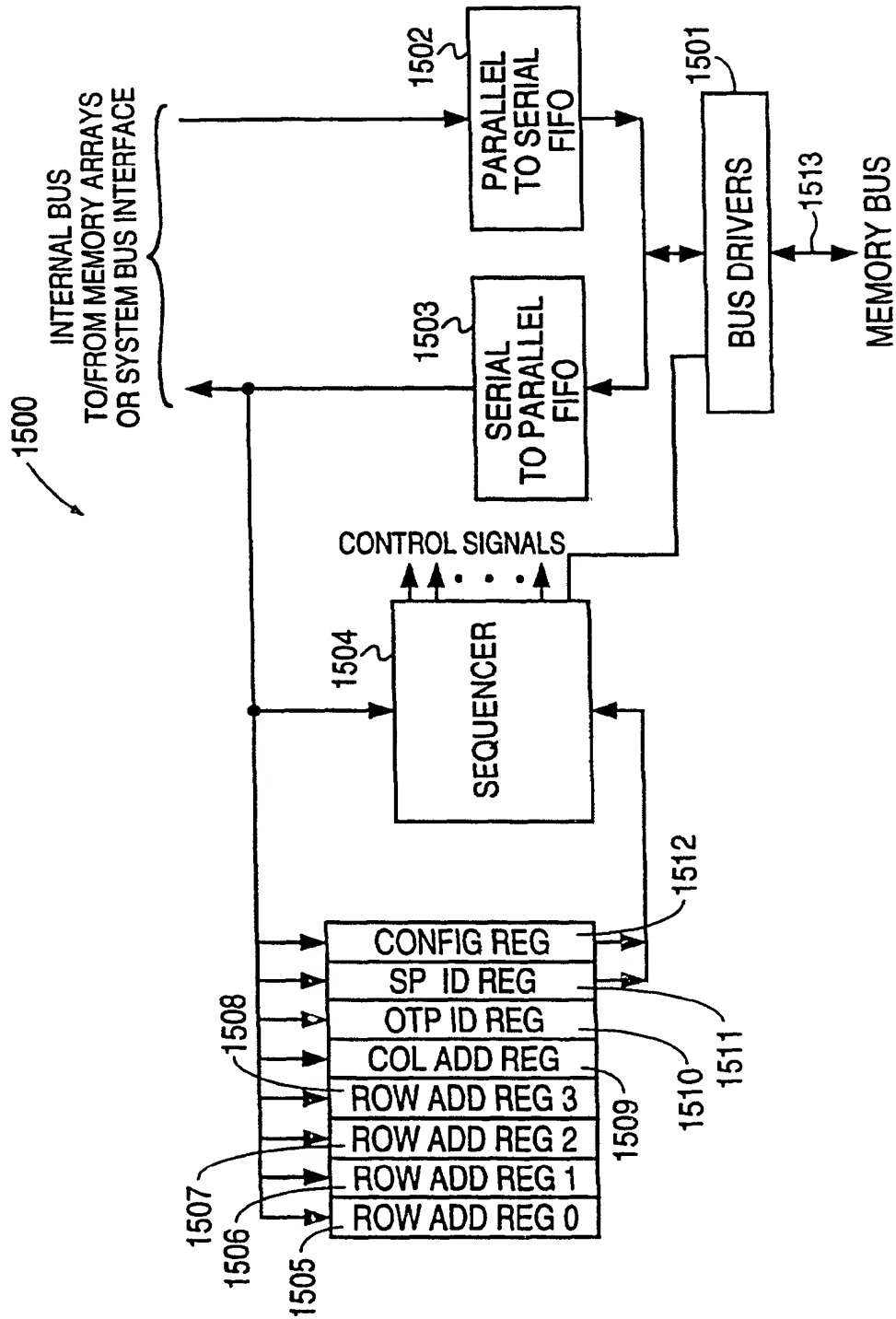


FIG. 15

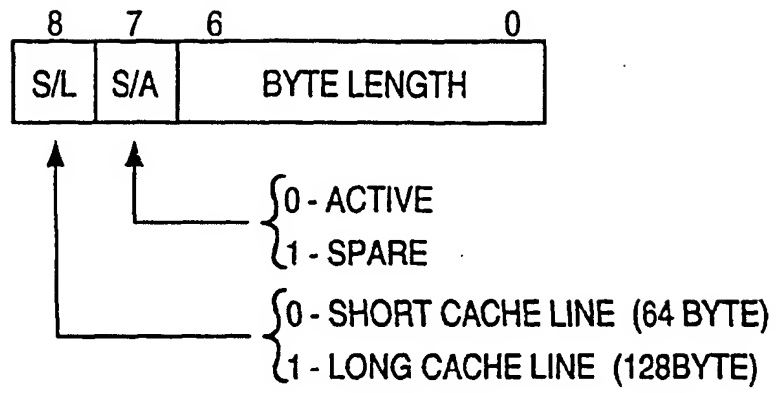


FIG. 16

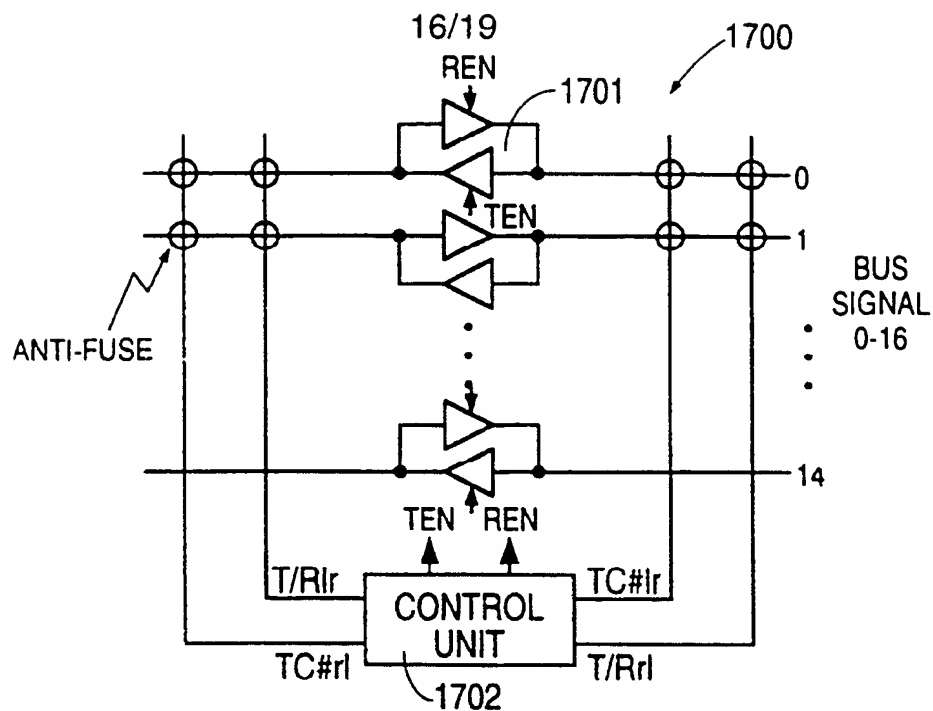


FIG. 17A

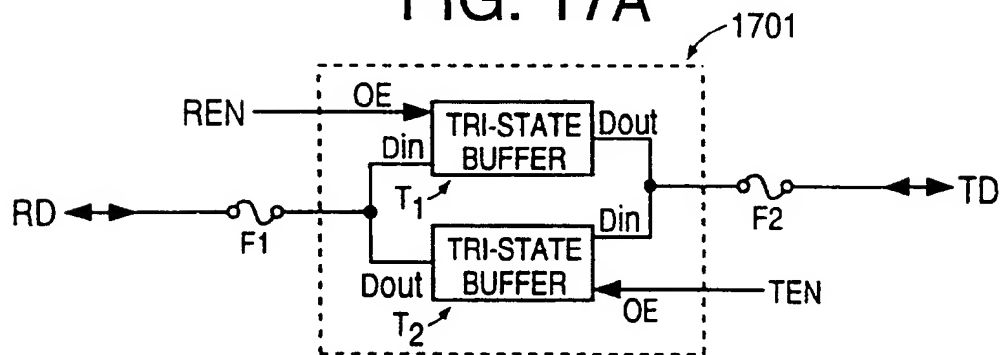


FIG. 17B

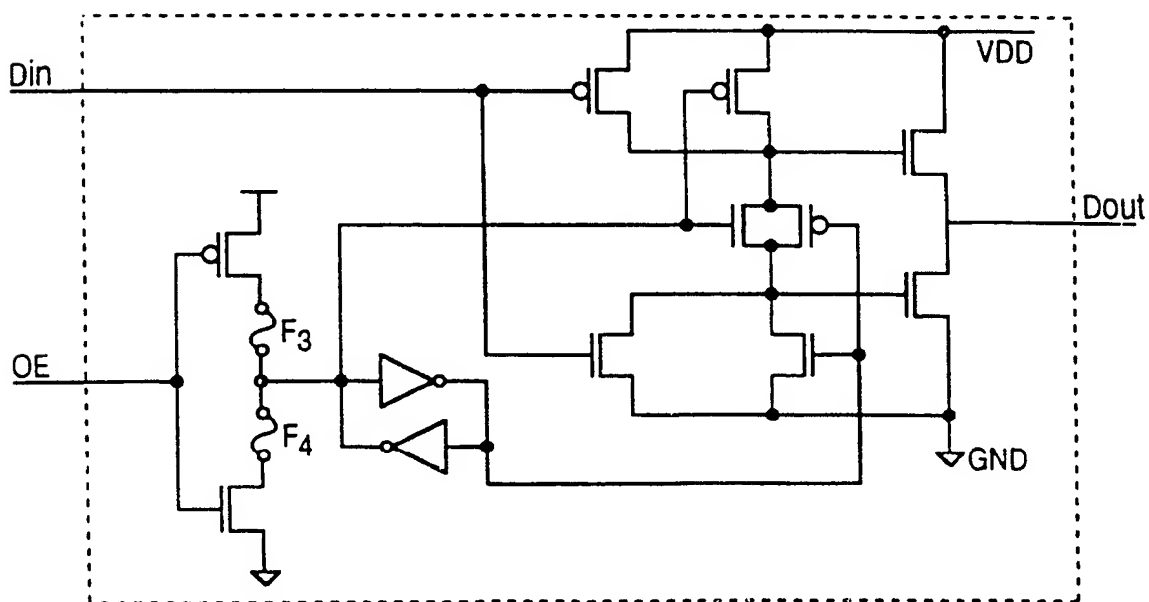


FIG. 17C

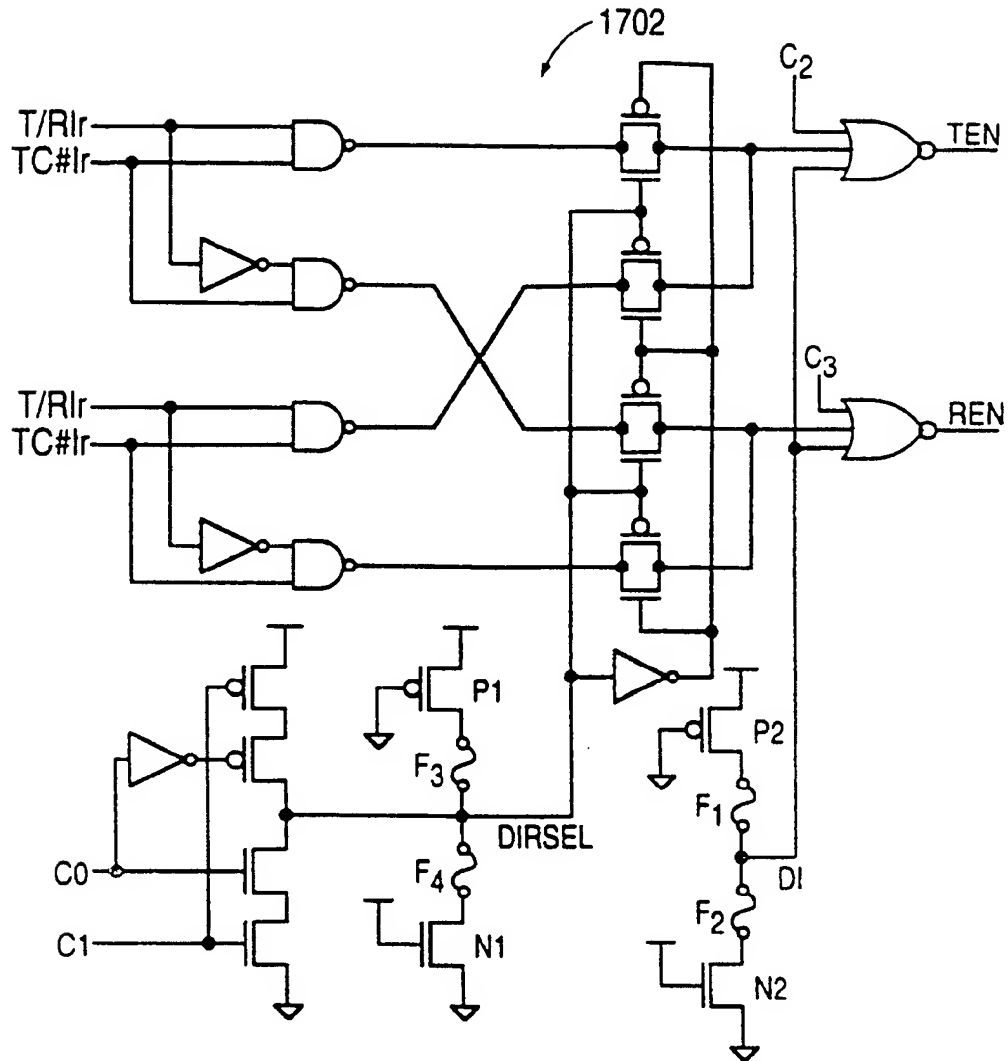


FIG. 17D

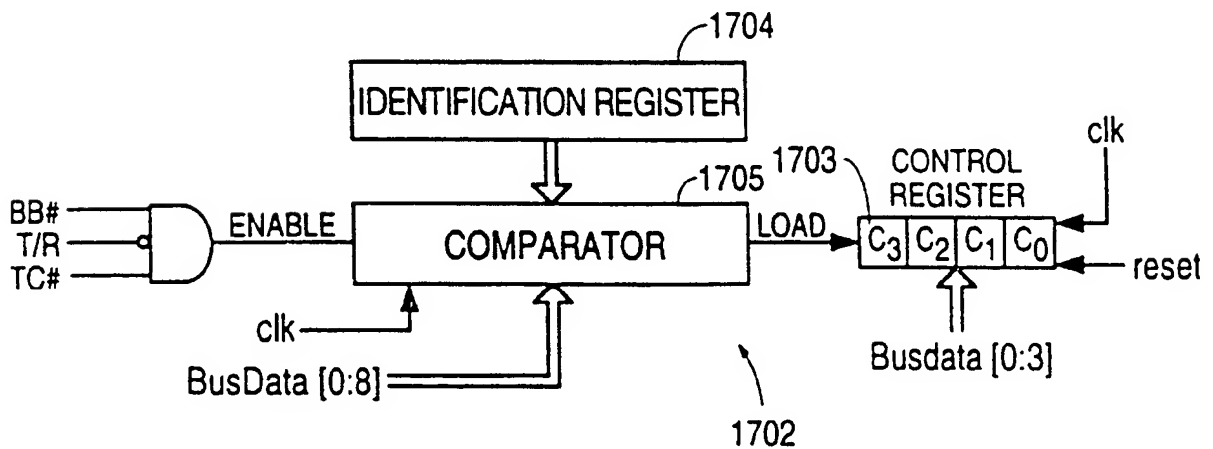


FIG. 17E

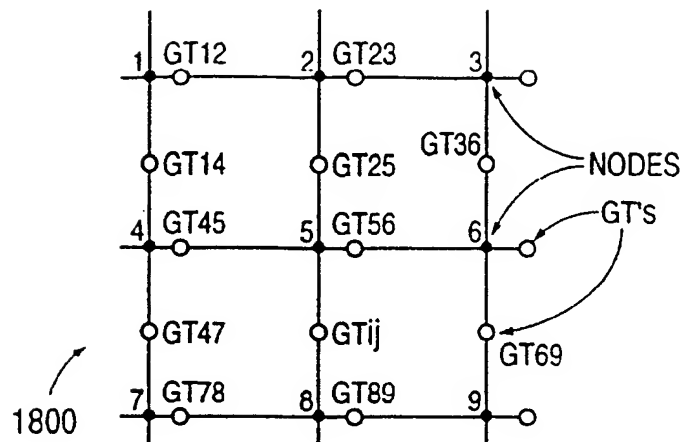


FIG. 18A

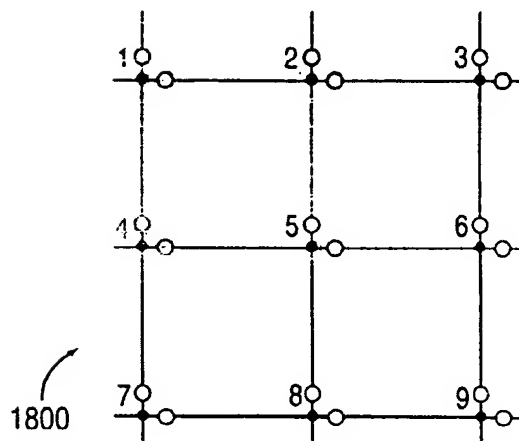


FIG. 18B

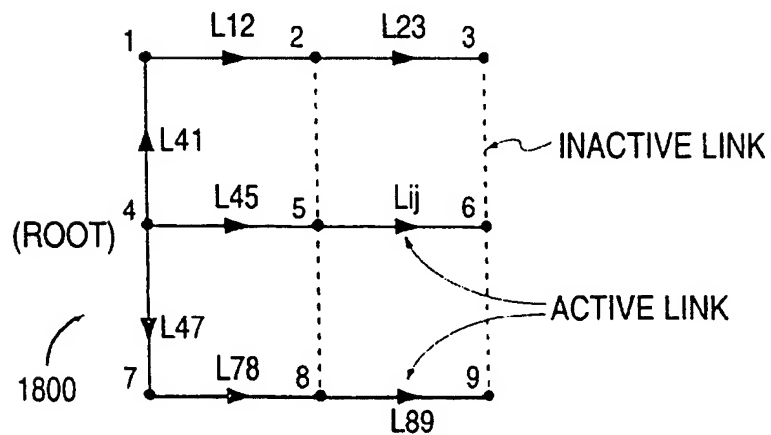


FIG. 18C

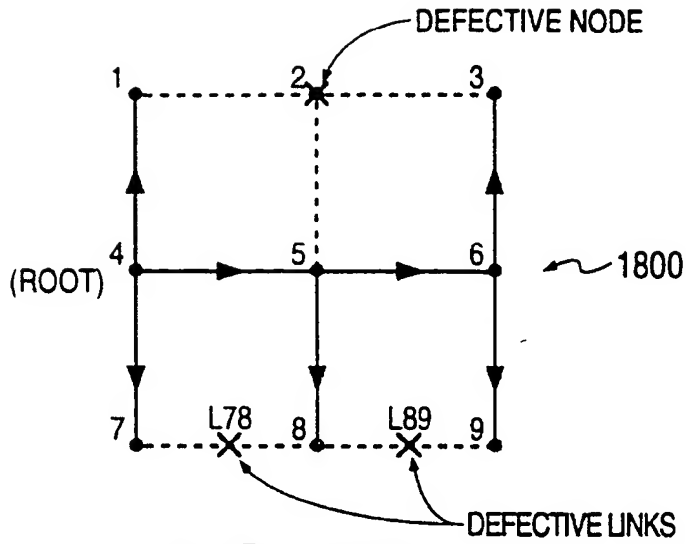


FIG. 18D

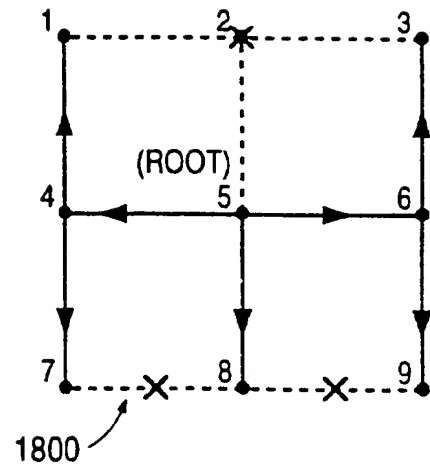


FIG. 18E

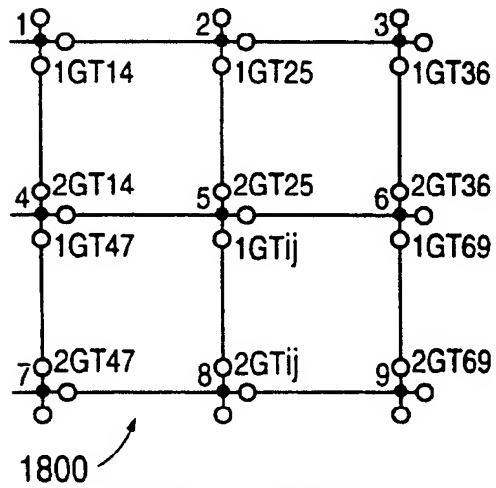


FIG. 18F

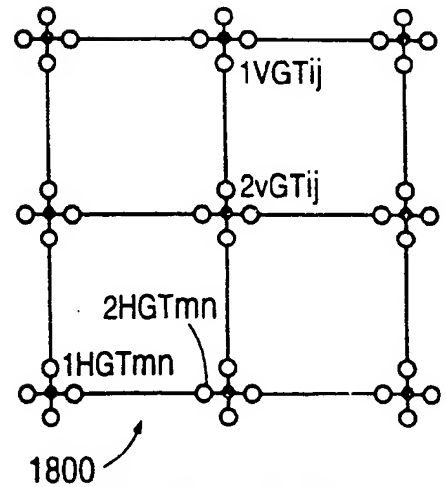


FIG. 18G